## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1 – 48 (canceled).

49. (previously presented) An integrated circuit (IC) including a plurality of field effect transistors (FETs) disposed on a semiconductor substrate, each of said FETs comprising:

a silicon device channel;

a gate disposed above said silicon device channel;

a source/drain extension laterally formed less than 100Å thick on an angled undercut following a silicon crystal (111) crystallographic plane and disposed at said each end of said silicon device channel; and

a portion of a low resistance material layer forming a smooth interface with and directly contacting a corresponding said source/drain extension.

50. (previously presented) An IC as in claim 49, wherein said low resistance material layer is a silicide layer.

51. (previously presented) An IC as in claim 50, wherein said semiconductor substrate is a silicon on insulator (SOI) substrate, each said gate is polysilicon and said plurality of FETs comprise a plurality of p-type FETs (PFETs) and a plurality of n-type FETs (NFETs) connected together in a circuit.

52. (previously presented) An IC as in claim 51, wherein said smooth silicide/silicon interface has a roughness of less than 100Å, whereby said corresponding source/drain extensions are free from silicide spiking.

53. (previously presented) An IC as in claim 52, wherein said silicide is a silicide of a material selected from a group of materials consisting of a silicide of tungsten (WSi), cobalt (CoSi), nickel (NiSi), titanium (TiSi), platinum (PtSi) and Erbium (ErSi).

54. (previously presented) An IC as in claim 53, wherein said silicide is selected from the group of metals consisting of WSi, NiSi and CoSi.

55. (previously presented) An IC as in claim 50, wherein said semiconductor substrate is a bulk silicon substrate, each said gate is polysilicon and said plurality of FETs comprise a plurality of p-type FETs (PFETs) and a plurality of n-type FETs (NFETs) connected together in a circuit.